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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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01/18/2001

Laurence H. Cooke

260/086

8269

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7590

11/17/2004

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EXAMINER

DIMYAN, MAGID Y

ART UNIT

PAPER NUMBER

2825

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/765,917

Applicant(s)

COOKE ET AL.

Examiner

Magid Y Dimyan

Art Unit

2825

Am

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 January 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) is/are withdrawn from consideration.
- 5) ☐ Claim(s) is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) is/are objected to.
- 8) ☒ Claim(s) 9-12 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 January 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. .
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. <u> </u> |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>4,6,8,9</u> . | 6) <input type="checkbox"/> Other: <u> </u> |

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C.

121:

I. Claims 1 – 8 (Group I), drawn to a circuit for a state machine to perform as a target and an initiator of a communication comprising a plurality of pins corresponding to target signals handling communication involving the component as a target, and a set of initiator signals handling communication involving the component as an initiator, classified in class 716, subclass 1.

II. Claims 9 - 10 (Group II), drawn to an IC and a model of an IC comprising a bus, functional blocks, ports connected to the bus, wherein each port is designed to perform both as a target and an initiator of a communication, classified in class 716, subclass 1.

II. Claims 11 - 12 (Group III), drawn to a method of designing an IC comprising specifying a communication block that includes locations of androgynous interfaces in the IC and setting the androgynous interfaces to perform as targets or initiators based on layout, classified in class 716, subclass 8.

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The inventions are distinct, each from the other because of the following reasons:

Inventions Group I, Group II and Group III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I has a separate utility such as an interface for communicating between electronic components comprising a circuit for a state machine to perform as a target and an initiator; invention Group II has a separate utility such as an IC and an IC model comprising a bus, functional blocks, ports connected to the bus, wherein the ports are designed to perform as both a target and an initiator of communication; and invention Group III has a separate utility such as a method of designing an IC comprising specifying a communication block that includes the locations of androgynous interfaces and setting the androgynous interfaces to perform as targets and initiators based on the layout. See MPEP § 806.05(d).

2. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their divergent subject matter, restriction for examination purposes as indicated is proper.
3. During a telephone conversation with the Applicants' attorney Mr. Peter Mei (Reg. No. 39,768) on 08 November 2004, a provisional election was made without traverse to prosecute the invention of Group I (Claims 1 – 8). Affirmation

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of this election must be made by the applicants in replying to this Office Action.

Groups II and III (Claims 9 - 12) are withdrawn from further consideration by the

examiner, 37 CFR 1.142(b), as being drawn to non-elected inventions. The

Applicants are requested to cancel claims 9 - 12 in the next office

communication.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 – 8 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,784,291 to Chen et al. (hereinafter, "Chen").

6. Referring to claim 1, Chen discloses an interface for communicating between electronic components having multiple connection points (see Fig. 9) comprising: (a) a circuit for a state machine to perform as a target and an initiator of communication (see Fig. 9; col. 19, lines 17 – 32; col. 80, lines 23 – 59; col. 88, lines 39 - 46); and (b) a plurality of pins connected to the circuit wherein the pins corresponding to a set of pins handling communications involving the

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component as a target and a set of initiator signals handling communication involving the component as an initiator (see MPU 102 – Figs. 5 and 9; col. 80, line 23 to col. 81, line 50). Thus, Chen cites all the claimed elements.

7. As to claims 2 and 3, see Figs. 5 and 9 which show which show the interface containing unidirectional pins with at least one input pin and one output pin, and also show the circuit with equal number of input pins and output pins, as claimed.

8. As per claim 4, see col. 65, line 56 to col. 66, line 23 which teach the MPU 102 with an integrated PCI bus interface with master/slave operation that supports both asymmetric as well as symmetric DRAM's (i.e., the set of target signals is symmetric with a set of initiator signals, as claimed).

9. Claims 5, 6, 7 and 8 contain the same limitations as claims 1, 2, 3 and 4, respectively, and thus the same rejections apply.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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U.S. Patent No. 6,122,690 to Nannetti et al. discloses a bus in an IC that uses bus interfaces to couple functional blocks to the bus in a processor independent and scalable manner, whereas the bus interfaces include a bus interface for a bus master functional block, a bus interface for a slave functional block, and a bus interface for either a bus master functional block or a slave functional block. Each bus interface includes a state machine.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Magid Y Dimyan
Examiner
Art Unit 2825

myd
10 November 2004

HYD

Abusando
Primary examiner
11/10/2004